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Title of the Invention	Method for Fabricating Contact Holes in a Semiconductor Device
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(transliterated, therefore the spelling might be incorrect)

[Title of the Invention] Method for Fabricating Contact Holes in a Semiconductor Device

[Claims]

[Claim 1]

A method for fabricating contact holes in a semiconductor

device comprising:

a first step of forming a first insulating film on a substrate provided with a first region and a second region, said first region including a high-melting-point metal layer or a silicide layer provided at least on the upper surface thereof, said second region including a high-melting-point metal layer or a silicide layer provided at least on the upper surface thereof, and said first insulating film having an etch selectivity with respect to said first region and said second region;

a second step of forming, on said first insulating film, a second insulating film having an etch selectivity with respect to said first insulating film and having different film thicknesses on said first region and on said second region;

a third step of forming a first upper contact hole through said second insulating film on said first region and forming a second upper contact hole through said second insulating film on said second region; and

a fourth step of forming a first lower contact hole through said first insulating film such that it is continuous with said first upper contact hole and forming a second lower contact hole through said first insulating film such that it is continuous with said second upper contact hole.

[Claim 2]

A method for fabricating contact holes in a semiconductor

device described in Claim 1, wherein said first region is wiring, an electrode or a diffusion layer formed on said substrate and said second region is wiring, an electrode or a diffusion layer formed on said substrate.

[Claim 3]

A method for fabricating contact holes in a semiconductor device described in Claim 1, wherein said first region is formed on the upper portion of a step on said substrate and said second region is formed on the bottom portion of a step on said substrate.

[Claim 4]

A method for fabricating contact holes in a semiconductor device described in Claim 3, wherein said first region is wiring, an electrode or a diffusion layer formed on the upper portion of a step on said substrate and said second region is wiring, an electrode or a diffusion layer formed on the bottom portion of a step on said substrate.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application]

The present invention relates to a method for fabricating contact holes provided in an insulating film, such as an interlayer insulating film, in a semiconductor device.

[0002]

[Prior Art]

An item required for high-speed devices is reduction in the wiring resistance. There is a technique for silicidizing the polycrystalline silicon used in the gate electrode and the source/drain diffusion layers for reducing the resistance. Particularly, the technique for silicidizing, in a self-aligning manner, the upper portion of the gate electrode and the upper portions of the source/drain diffusion layers, is called a salicide technique.

[0003]

On the other hand, aluminum-based metals are mainly employed as the wiring material in steps requiring no high-temperature heat treatment after the formation of transistors. In recent years, multiple layers of wiring have been utilized in view of the integration degree. However, aluminum-based wiring can not achieve sufficient step coverage, thus requiring flat interlayer insulating films for preventing breakage of wiring. Furthermore, due to the insufficient margin of the focal depth in lithography processes for large steps, there is a need for flat interlayer insulating films.

[0004]

With reference to the views of fabrication steps in Fig. 4, there will be described an exemplary formation of contact holes in an interlayer insulating film on the gate electrode and an interlayer insulating film on the diffusion layer, in the case of combining the aforementioned salicide technique and

flat interlayer insulating films.

[0005]

As illustrated in Fig. 4(1), a gate electrode 113 is formed on a substrate 111 with a gate insulating film 112 interposed therebetween. Further, source/drain diffusion layers 114, 115 are formed on the substrate 111 at the both sides of the gate electrode 113. Further, silicide layers 116, 117, 118 are formed on the gate electrode 113 and on the source/drain regions 114, 115, respectively. An interlayer insulating film 121 is formed on this substrate 111. Further, in the figure, there are also illustrated device separation regions and side walls provided on the side wall of the gate electrode.

[0006]

Subsequently, as illustrated in Fig. 4(2), by a lithography technique and etching, contact holes 122, 123, 124 are formed in the interlayer insulating film 121 on the gate electrode 113 and on the source/drain diffusion layers 114, 115, wherein the contact holes 122, 123, 124 are communicated with the gate electrode 113 and the source/drain diffusion layers 114, 115, respectively. The illustration of the resist mask is omitted in the figure.

[0007]

[Problems to be Solved by the Invention]

However, with the aforementioned fabrication method of contact holes, as illustrated in Fig. 5, the interlayer

insulating film 121 is thicker on the source/drain diffusion layers 114, 115 than on the gate electrode 113. Therefore, when the contact holes 122, 123, 124 are formed concurrently through the interlayer insulating layers 121 on the gate electrode 113 and on the source/drain diffusion layers 114, 115, the formation of the contact hole 122 on the gate electrode 113 will be completed earlier. Further, the formation of the contact holes 123, 124 on the source/drain regions 114, 115 is continued even after the completion of the formation of the contact hole 122, and this etching causes excessive etching of the bottom portion of the contact hole 122. As a result, the silicide layer 116 formed on the upper portion of the gate electrode 113 is etched, thus resulting in degradation of the resistance reducing effect of the silicide layer 116 for the gate electrode 113.

[0008]

It is an object of the present invention to provide a method for forming contact holes in a semiconductor device which is advantageous in forming contact holes through an insulating film having different film thicknesses without causing etching of the underlying material.

[0009]

[Means for Solving Problems]

The present invention is a fabrication method of contact holes in a semiconductor device for achieving the aforementioned object. Namely, in a first step, a first

insulating film is formed on a substrate provided with a first region and a second region, the first region including a high-melting-point metal layer or a silicide layer provided at least on the upper surface thereof, the second region including a high-melting-point metal layer or a silicide layer provided at least on the upper surface thereof, and the first insulating film having an etch selectivity with respect to the first region and said second region, respectively. Subsequently, in a second step, a second insulating film is formed on the first insulating film, wherein the second insulating film has an etch selectivity with respect to the first insulating film and has different film thicknesses on the first region and on the second region. In the third step, a first upper contact hole is formed through the second insulating film on the first region and a second upper contact hole is formed through the second insulating film on the second region. Then, in a fourth step, a first lower contact hole is formed through the first insulating film such that it is continuous with the first upper contact hole and a second lower contact hole is formed through the first insulating film such that it is continuous with the second upper contact hole.

[0010]

[Effects]

With the aforementioned fabrication method of contact holes in a semiconductor device, the etching of the second

insulating film having an etch selectivity is stopped at the upper portion of the first insulating film in forming contact holes through the second insulating film, since the first insulating film is provided. Therefore, even when the second insulating film has different thicknesses on the first and second regions, the etching is stopped at the upper portion of the first insulating film. Then, the first insulating film is etched to form the first lower contact hole continuous with the first upper contact hole and the second lower contact hole continuous with the second upper contact hole. At this time, since the first insulating film has an etch selectivity with respect to the first and second regions, the first insulating film is etched almost without etching the first and second regions. Thus, the first and second lower contact holes are formed almost without etching the first and second regions.

[0011]

[Embodiments]

A first embodiment of the present invention will be described with reference to the views of fabrication steps.

[0012]

As illustrated in Fig. 1(1), a first region 12 and a second region 13 are provided on a substrate 11. The first region 12 is, for example, wiring formed on the substrate 11 and a silicide layer 14 is formed on the upper surface thereof. Instead of the silicide layer 14, a high-melting-point metal layer may be

employed. The second region 13 is, for example, a diffusion layer formed on the substrate 11 and a silicide layer 15 is formed on the upper surface thereof. Instead of the silicide layer 15, a high-melting-point metal layer may be employed.

[0013]

At first, in a first step, by a low pressure chemical vapor deposition (hereinafter, referred to as LPCVD) process, a first insulating film 16 with an etch selectivity with respect to the first and second regions 12, 13 (for example, the selection ratio therebetween is equal to or more than about 3 to 5) is formed on the substrate 11 such that it covers the first and second region 12, 13. The first insulating film 16 is formed from, for example, a silicon nitride film. The etch selectivity ratio of the high-melting-point metal or the silicide with respect to the silicon nitride is about 10.

[0014]

In the aforementioned LPCVD process, for example, a common LPCVD apparatus was utilized as the apparatus. As the reactant gases, for example, dichlorosilane (SiH_2Cl_2) at a flow rate of 50 sccm, ammonia (NH_3) at a flow rate of 200 sccm and nitrogen (N_2) at a flow rate of 2000 sccm were employed. Further, the pressure of the reactive atmosphere was set to, for example, 70 Pa and the temperature of the substrate was set to, for example, 760°C. Instead of LPCVD, a plasma chemical vapor deposition (hereinafter, referred to as plasma CVD) process may be utilized.

In the case of film deposition utilizing a plasma CVD process, a common parallel-plate single-wafer type plasma CVD apparatus is utilized as the film deposition apparatus and mono-silane (SiH_4) at a flow rate of 50 sccm, ammonia (NH_3) at a flow rate of 200 sccm and nitrogen (N_2) at a flow rate of 2000 sccm are employed, for example, as the reactant gases. Further, the pressure of the reactive atmosphere is set to, for example, 600 Pa and the temperature of the substrate is set to, for example, 360°C.

[0015]

Subsequently, a second step illustrated in Fig. 1(2) is performed. In this step, by a normal-pressure chemical vapor deposition (hereinafter, referred to as normal-pressure CVD) process, a second insulating film 17 having an etch selectivity with respect to the first insulating film 16 (for example, the etch selection ratio therebetween is equal to or more than about 3 to 5) is formed on the aforementioned first insulating film 16. The second insulating film 17 is formed from, for example, phosphorus silicate glass (hereinafter, referred to as PSG) and is formed such that the surface thereof is flat. Further, the first region 12 is formed to be higher than the second region 13. Therefore, the second insulating film 17 has a greater thickness on the second region 13 than on the first region 12.

[0016]

Subsequently, a third step illustrated in Fig. 1(3) is

performed. In this step, by a lithography technique (resist coating, exposure, development, baking, etc.), a resist mask 31 is formed on the second insulating film 17 and openings 32, 33 are formed above the first and second regions 12, 13. Then, by reactive ion etching (hereinafter, referred to as RIE), for example, the second insulating film 17 is etched until the aforementioned second insulating film 16 is exposed. Then, a first upper contact hole 18 is formed through the second insulating film 17 on the first region 12 and a second upper contact hole 19 is formed through the second insulating film 17 on the second region 13.

[0017]

In the aforementioned RIE, for example, a common single-wafer type magnetron RIE apparatus was employed as the etching apparatus. As the etching gases, for example, octafluorocyclobutane (C_4F_8) at a flow rate of 8 sccm and carbon monoxide (CO) at a flow rate of 60 sccm were employed. As the carrier gas, for example, argon (Ar) at a flow rate of 200 sccm was employed. The pressure of the etching atmosphere was set to, for example, 5.3 Pa and the high-frequency electric power was set to, for example, 1.6 kW. The temperature of the suscepter , as the substrate temperature, was set to 30°C, for example.

[0018]

Subsequently, a fourth step illustrated in Fig. 1(4) is

performed. In this step, by RIE, for example, a first lower contact hole 20 is formed through the first insulating film 16 such that it is continuous with the first upper contact hole 18 and a second lower contact hole 21 is formed through the first insulating film 16 such that it is continuous with the second upper contact hole 19. Thus, a first contact hole 22 is constituted by the first upper contact hole 18 and the first lower contact hole 20 and a second contact hole 23 is constituted by the second upper contact hole 19 and the second lower contact hole 21.

[0019]

In the RIE, in the case where the aforementioned silicide layer 14 and the silicide layer 15 are made from, for example, titanium silicide, a common single-wafer type magnetron RIE apparatus was employed as the etching apparatus. As the etching gases, for example, octafluorocyclobutane (C_4F_8) at a flow rate of 30 sccm and carbon monoxide (CO) at a flow rate of 170 sccm were employed. The pressure of the etching atmosphere was set to, for example, 5.3 Pa and the high-frequency electric power was set to, for example, 1.0 kW. The temperature of the suscepter , as the substrate temperature, was set to 30°C, for example.

[0020]

Subsequently, the etching mask 31 used in the aforementioned RIE is removed, by oxygen-plasma ashing or wet

processing using a remover liquid.

[0021]

In the aforementioned fabrication method of contact holes in a semiconductor device, the first insulating film 16 is formed and then the second insulating film 17 having an etch selectivity with respect to the first insulating film 16 is formed on the upper surface of the first insulating film 16. Consequently, in etching the second insulating film 17 to form the first and second upper contact holes 18, 19, the etching thereof is stopped at the upper portion of the first insulating film 16 even when the second insulating film 17 has different film thicknesses on the first and second regions 12, 13. Subsequently, the first insulating film 16 having an etch selectivity with respect to the first and second regions 12, 13 is etched and thus the first and second lower contact holes 20, 21 are formed almost without etching the first and second regions 12, 13. Consequently, the first and second contact holes 23, 23 are formed almost without etching the first and second regions 12, 13.

[0022]

In the aforementioned first embodiment, it is not necessary that the aforementioned first region 12 is wiring and it may be an electrode or a diffusion layer formed on the substrate 11. Further, it is not necessary that the aforementioned second region 13 is a diffusion layer and it may

be wiring or an electrode. Further, while the aforementioned first embodiment has been described with respect to the case where the first insulating films 16 is made of silicon nitride and the second insulating film 17 is made of PSG, they are not limited to these materials and may be any materials having an etch selectivity with respect to the underlying material. Further, while the second insulating film 17 has been described as being a flat film, it may be any film having different thicknesses on the first and second regions 12, 13 and is not required to be a flat film. Also, the second insulating film 17 may have a construction consisting of plural laminated insulating films. Further, the fabrication method according to the present invention may be utilized even when the second insulating film 17 has substantially the same thickness on the first and second regions 12, 13.

[0023]

Hereinafter, with reference to views of fabrication steps in Fig. 2, there will be described concrete exemplary applications of the aforementioned fabrication method of contact holes to a semiconductor device. In the figure, there is illustrated, as an example, a metal-insulating film-semiconductor (hereinafter, referred to as MIS) transistor.

[0024]

As illustrated in Fig. 2(1), a gate electrode 53

(corresponding to the first region 12 in Fig. 1) is formed on a silicon substrate 51 (corresponding to the substrate 11 in Fig. 1) with a gate insulating film 52 interposed therebetween. The gate electrode 53 has a so-called polycide construction and includes a lower layer formed from a polycrystalline silicon layer 54 and an upper layer formed from, for example, a titanium silicide layer 55. Further, on the silicon substrate 51, there are formed source/drain regions 56, 57 (corresponding to the second region 13 in Fig. 1), at the both sides of the gate electrode 53. Titanium silicide layers 58, 59 are formed on the source/drain regions 56, 57. Namely, the MIS transistor 50 configured as above has a salicide construction. Further, in the figure, there are also illustrated device separation regions and side walls provided on the side walls of the gate electrode 53.

[0025]

In a first step, for example, by an LPCVD process or a plasma CVD process, a first insulating film 16 with an etch selectivity with respect to the aforementioned titanium silicide layers 55, 58, 59 (for example, the selection ratio therebetween is equal to or more than about 3 to 5) is formed on the substrate 51 such that it covers the aforementioned gate electrode 53. The first insulating film 16 is formed from, for example, a silicon nitride film. In the LPCVD process or the plasma CVD process, the deposition of a silicon nitride film

is performed under a condition similar to that described with respect to Fig. 1.

[0026]

Subsequently, a second step illustrated in Fig. 2(2) is performed. In this step, by a normal-pressure CVD process, a second insulating film 17 having an etch selectivity with respect to the first insulating film 16 (for example, the etch selection ratio therebetween is equal to or more than about 3 to 5) is formed on the first insulating film 16. The second insulating film 17 is made of, for example, phosphorus silicate glass (hereinafter, referred to as PSG) and is formed such that the surface thereof is flat. Therefore, the second insulating film 17 has different film thicknesses on the gate electrode 53 and on the source/drain regions 56, 57. In this case, the second insulating film 17 has a greater thickness on the source/drain regions 56, 57 than on the gate electrode 53.

[0027]

Subsequently, in a third step illustrated in Fig. 2(3), an etching mask 60 is formed by a lithography technique (resist coating, exposure, development, baking, etc.) and then the second insulating film 17 is etched by RIE until the aforementioned second insulating film 16 is exposed. Then, a first upper contact hole 61 is formed through the second insulating film 17 on the gate electrode 53 and second upper contact holes 62, 63 are formed through the second insulating

film 17 on the source/drain regions 56, 57. In the RIE, the etching is performed under a condition similar to that described with respect to Fig. 1.

[0028]

Then, in a fourth step illustrated in Fig. 2(4), by RIE, a first lower contact hole 64 is formed through the first insulating film 16 such that it is continuous with the first upper contact hole 61 and second lower contact holes 65, 66 are formed through the first insulating film 16 such that they are continuous with the second upper contact holes 62, 63. Thus, a first contact hole 67 communicated with the gate electrode 53 is constituted by the first upper contact hole 61 and the first lower contact hole 64 and second contact holes 68, 69 communicated with the source/drain regions 56, 57 are constituted by the second upper contact holes 62, 63 and the second lower contact holes 65, 66. In the RIE, the etching is performed under a condition similar to that described with respect to Fig. 1.

[0029]

Subsequently, the etching mask 60 used in the aforementioned RIE is removed by oxygen-plasma ashing or wet processing using remover liquid.

[0030]

As described above, the contact holes 67, 68, 69 can be formed almost without etching the titanium silicide layer 55

in the gate electrode 53 and the titanium silicide layers 58, 59 on the source/drain regions 56, 57. Consequently, the resistance reducing effect provided by the titanium silicide layers 55, 58, 59 will not be degraded. This enables ensuring high-speed operations of semiconductor devices such as static RAMs [SRAM (Static Random Access Memories)] or ASICs (Application Specific Integrated Circuits) equipped with MIS transistors having a salicide construction, without causing reduction in the operation speed.

[0031]

Next, a second embodiment will be described with reference to the views of fabrication steps in Fig. 3. Components similar to those described in the Fig. 1 are designated by the same reference characters.

[0032]

As illustrated in Fig. 3(1), on a substrate 71 with a step, a first region 12 is formed on the upper portion 71U of the step and a second region 13 is formed in the bottom portion 71B of the step. The first region 12 is, for example, wiring formed on the substrate 71 and a silicide layer 14 is formed on the upper surface thereof. A high-melting-point metal layer may be provided instead of the silicide layer 14. The second region 13 is, for example, a diffusion layer formed on the substrate 71 and a silicide layer 15 is formed on the upper surface thereof. A high-melting-point metal layer may be provided instead of the

silicide layer 15.

[0033]

Similarly to the description with respect to Fig. 1, in a first step, a first insulating film 16 having an etch selectivity with respect to the first and second regions 12, 13 (for example, the selectivity ratio therebetween is equal to or more than about 3 to 5) is formed on the substrate 71 such that it covers the first and second region 12, 13.

[0034]

Subsequently, in a second step, a second insulating film 17 having an etch selectivity with respect to the first insulating film 16 (for example, the etch selection ratio therebetween is equal to or more than about 3 to 5) is formed on the first insulating film 16. In this case, the second insulating film 17 is formed from, for example, phosphorus silicate glass (hereinafter, referred to as PSG) such that the surface thereof is flat. Further, the first region 12 is higher than the second region 13. Consequently, the second insulating film 17 has a greater thickness on the second region 13 than on the first region 12.

[0035]

Subsequently, in a third step illustrated in Fig. 3(2), by a lithography technique and, for example, RIE, the second insulating film 17 is etched until the aforementioned first insulating film 16 is exposed. Then, a first upper contact hole

18 is formed through the second insulating film 17 on the first region 12 and a second upper contact hole 19 is formed through the second insulating film 17 on the second region 13. Since the second insulating film 17 has an etch selectivity with respect to the first insulating film 16, the etching thereof is stopped at the upper portion of the first insulating film 16. In the figure, the illustration of the resist mask is omitted.

[0036]

Then, in a fourth step illustrated in Fig. 3(3), by RIE, a first lower contact hole 20 is formed through the first insulating film 16 such that it is continuous with the first upper contact hole 18 and a second lower contact hole 21 is formed through the first insulating film 16 such that it is continuous with the second upper contact hole 19. Thus, a first contact hole 22 is constituted by the first upper contact hole 18 and the first lower contact hole 20 and the second contact hole 23 is constituted by the second upper contact hole 19 and the second lower contact hole 21. Since the first insulating film 16 has an etch selectivity with respect to the first and second regions 12, 13, the etching thereof is stopped at the upper portions of the first and second regions 12, 13.

[0037]

With the fabrication method of contact holes which has been described with reference to Fig. 3, the first and second

contact holes 22, 23 can be formed almost without etching the first and second regions 12, 13, similarly to the fabrication method of contact holes described with reference to Fig. 1.

[0038]

In the aforementioned second embodiment, it is not necessary that the aforementioned first region 12 is wiring and it may be, for example, an electrode or a diffusion layer formed on the substrate 71. Further, it is not necessary that the aforementioned second region 13 is a diffusion layer and it may be, for example, wiring or an electrode. Further, while the aforementioned second embodiment has been described with respect to the case where the first insulating films 16 is made of silicon nitride and the second insulating film 17 is made of PSG, they are not limited to these materials and may be any materials having an etch selectivity with respect to the underlying material. Further, while the second insulating film 17 has been described as being a flat film, it may be any film having different thicknesses on the first and second regions 12, 13 and is not required to be a flat film. Also, the second insulating film 17 may have a construction consisting of plural laminated insulating films. Further, the fabrication method according to the present invention may be utilized even when the second insulating film 17 has substantially the same thickness on the first and second regions 12, 13.

[0039]

[Effects of the Invention]

As described above, according to the present invention, there is provided the first insulating film having an etch selectivity with respect to the first and second regions which are underlying materials. Therefore, the etching of the second insulating film can be stopped at the first insulating film when forming contact holes through the second insulating film and also the first insulating film can be etched almost without etching the first and second regions to form the first and second contact holes. This enables ensuring the thickness of the layers under the first and second regions, thus preventing degradation in the performance of the semiconductor device.

[Brief Description of the Drawings]

Fig. 1 is views of fabrication steps according to the first embodiment of the present invention.

Fig. 2 is views of fabrication steps according to a concrete exemplary application according to the first embodiment.

Fig. 3 is views of fabrication steps according to the second embodiment.

Fig. 4 is views of fabrication steps according to an example of the prior art.

Fig. 5 is a view for explaining problems.

[Description of the Reference Characters]

11: substrate

12: first region

13: second region

14: silicide layer

15: silicide layer

16: first insulating film

17: second insulating film

18: first upper contact hole

19: second upper contact hole

20: first lower contact hole

21: second lower contact hole

22: first contact hole

23: second contact hole

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